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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/388,857	09/01/1999	LUAN C. TRAN	MI22-878	4528

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EXAMINER
SCHILLINGER, LAURA M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/388,857	TRAN, LUAN C.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 51-84* is/are pending in the application.

4a) Of the above claim(s) *75-84* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 51-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Paper No. 23, dated 5/5/03.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 and 51-74 are rejected under 35 U.S.C. 102(e) as being anticipated by Liaw et al ('276).

In reference to claim 1, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different widths and voltages (Table 1, Fig.4).

In reference to claim 2, Liaw et al teaches wherein there is no separate channel implant (Table 1, Fig.4).

In reference to claim 3, Liaw et al teaches wherein the widths are less than one micron (Col.2, lines: 1-10).

In reference to claim 4, Liaw et al teaches wherein the threshold voltages are less than 2 volts (Table 1, Fig.4).

In reference to claim 5, Liaw et al teaches wherein the threshold voltages are less than one volt (Table 1, Fig.4).

In reference to claim 6, Liaw et al teaches wherein the widths are less than one micron and the threshold voltages are less than 2 v (Table 1, Fig.4).

In reference to claim 7, Liaw et al teaches wherein the widths are less than one micron and the threshold voltages are less than 1 v (Table 1, Fig.4).

In reference to claim 51, Liaw et al teaches wherein one active area width is less than 1 um (Table 1, Fig.4).

In reference to claim 52, Liaw et al teaches wherein forming individual transistors comprises forming three individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4).

In reference to claim 53, Liaw et al teaches wherein forming individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4), the three individual transistors being configured to be coupled in parallel (Fig.3B).

In reference to claim 54, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different threshold voltages without using a separate channel implant (Table 1, Fig.4).

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4).

In reference to claim 55, Liaw et al teaches wherein the higher TV has an active area greater than 1 um (Table 1, Fig.4).

In reference to claim 56, Liaw et al teaches wherein the higher TV has an active area less than 1 um (Table 1, Fig.4).

In reference to claim 57, Liaw et al teaches wherein one common channel implant is conducted (Col.3, lines: 35-40).

In reference to claim 58, Liaw et al teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.3B).

In reference to claim 59, Liaw et al teaches wherein the gate line comprises a common gate line and the Ts are parallel (Fig. 3B).

In reference to claim 60, Liaw et al teaches wherein the TV are less than 1 V(Table 1, Fig.4).

In reference to claim 61, Liaw et al teaches wherein the widths are less than 1 um, and the TV are less than 2 V (Table 1, Fig.4).

In reference to claim 62, Liaw et al teaches wherein the widths are less than 1um and the TV are less than 1 V (Table 1, Fig.4).

In reference to claim 63, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas (Col.1, lines: 60-68), with some widths being no greater than 1 um, at least two being different (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different widths having different threshold voltages without using a separate channel implant (Table 1, Fig.4),wherein the different threshold voltages are each less than 2 volts (Table 1, Fig.4)

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4).

In reference to claim 64, Liaw et al teaches wherein the two widths are less than 1 um (Table 1, Fig.4).

In reference to claim 65, Liaw et al teaches wherein the TV are less than 1 v (Table 1, Fig.4)..

In reference to claim 66 Liaw et al teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Table 1, Fig.4).

In reference to claim 67, Liaw et al teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define a plurality of active areas having widths over the substrate (Col.1, lines: 60-68), with at least two of the widths being different and at least one of the plurality of widths being no greater than 1 um, (Col.2, lines: 1-10);

forming a transistor gate line over the active areas (Col.3-4, lines: 65-2) and, the transistor having different threshold voltages (Table 1, Fig.4), the transistors being provided with different threshold voltages without using a separate channel implant (Table 1, Fig.4), wherein the gate line comprises forming a gate line over the plurality of active areas, the transistor formed in parallel configuration (Fig.3B); and

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Table 1, Fig.4).

In reference to claim 68, Liaw et al teaches wherein the higher TV has an active area greater than 1 um (Table 1, Fig.4).

In reference to claim 69, Liaw et al teaches wherein the higher TV has an active area less than 1 um (Table 1, Fig.4).

In reference to claim 70, Liaw et al teaches wherein one common channel implant is conducted (Col.3, lines: 35-40).

In reference to claim 71, Liaw et al teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.3B).

In reference to claim 72, Liaw et al teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Table 1, Fig.4).

In reference to claim 73, Liaw et al teaches wherein the threshold voltages are less than 2 volts (Table 1, Fig.4).

In reference to claim 74, Liaw et al teaches wherein forming individual transistors, a first of the three having a first Tv, a second of the three having a second Tv, greater than the first Tv and a third of the three having a third Tv greater than the second Tv (Table 1, Fig.4), the three individual transistors being configured to be coupled in parallel (Fig.3B).

Response to Arguments

Applicant's arguments with respect to claims 1-7, 51-74 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS
July 26, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800